Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Q12**
2. **Q6**
3. **Q5**
4. **Q7**
5. **Q4**
6. **Q3**
7. **Q2**
8. **GND**
9. **Q1**
10. **Ø**
11. **MR**
12. **Q9**
13. **Q8**
14. **Q10**
15. **Q11**
16. **VCC**

**.068”**

**HC4040**

**MASK**

**REF**

**10 9 8 7**

**11**

**12**

**13**

**14**

**6**

**5**

**4**

**3**

**15 16 1 2**

**A**

**.071”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: HC4040 A**

**APPROVED BY: DK DIE SIZE .068” X .071” DATE: 2/8/17**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54HC4040**

**DG 10.1.2**

#### Rev B, 7/19/02